AiP74LVC/LVCH4T774
4-bit Dual Supply Translating Transceiver; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2017-05-A1	2017-05	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The AiP74LVC/LVCH4T774 is a 4-bit, dual supply transceiver that enables bidirectional level translation. It features eight 1-bit input-output ports (An and Bn), four direction control inputs (DIR1, DIR2, DIR3 and DIR4), an output enable input ($\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2V and 5.5V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V). Pins An, $\overline{OE}$ and DIRn are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A HIGH on DIRn allows transmission from An to Bn and a LOW on DIRn allows transmission from Bn to An. The output enable input ($\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both An and Bn are in the high-impedance OFF-state.

Active bus hold circuitry in the AiP74LVCH4T774 holds unused or floating data inputs at a valid logic level.

Features:

- Wide supply voltage range:
  $V_{CC(A)}$: 1.2V to 5.5V
  $V_{CC(B)}$: 1.2V to 5.5V
- Suspend mode
- ±24mA output drive (V_{CC}=3.0V)
- Inputs accept voltages up to 5.5V
- Low power consumption: 30uA maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40℃ to +125℃
- Packaging information: SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVC4T774 SA16.TB	SOP16	74LVC4T774	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74LVCH4T774 SA16.TB	SOP16	74LVCH4T774	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74LVC4T774 TA16.TB	TSSOP16	74LVC4T774	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74LVCH4T774 TA16.TB	TSSOP16	74LVCH4T774	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVC4T774 SA16.TR	SOP16	74LVC4T774	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74LVCH4T774 SA16.TR	SOP16	74LVCH4T774	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74LVC4T774 TA16.TR	TSSOP16	74LVC4T774	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74LVCH4T774 TA16.TR	TSSOP16	74LVCH4T774	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

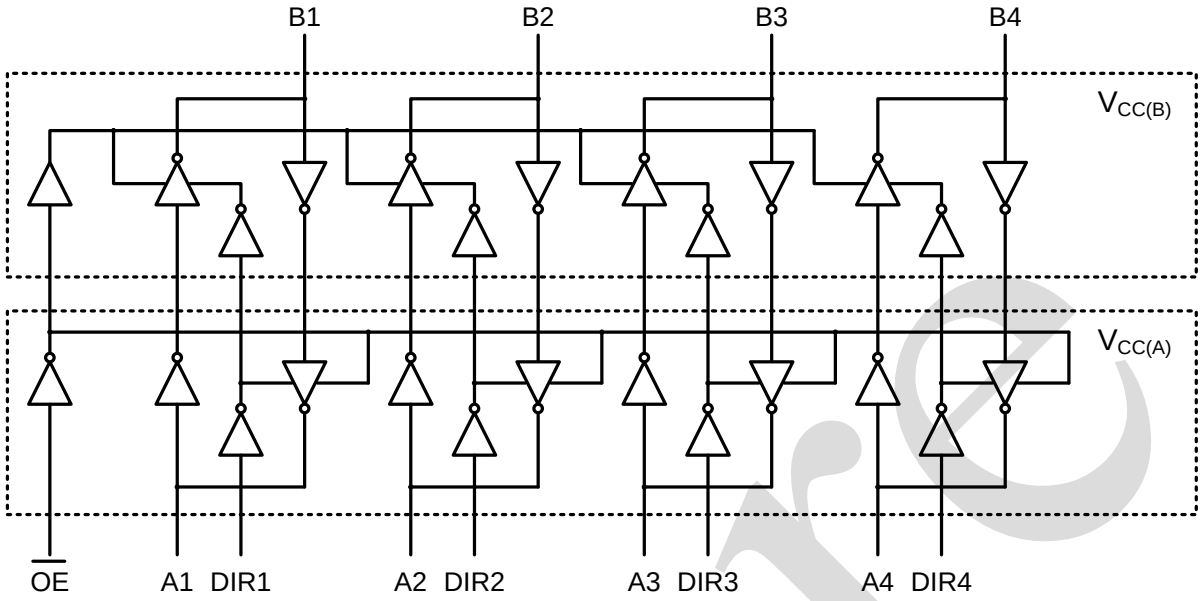


Figure 1. Logic symbol

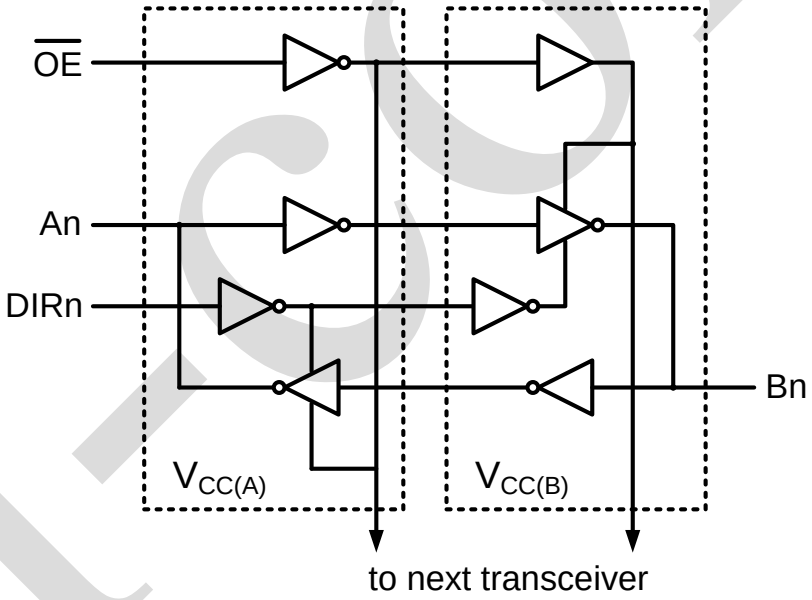
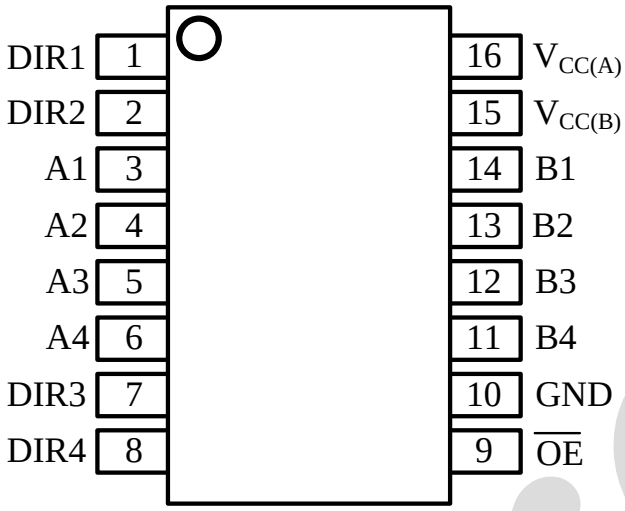


Figure 2. Logic diagram(one 1-bit transceiver)

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	DIR1	direction control input
2	DIR2	direction control input
3	A1	data input or output
4	A2	data input or output
5	A3	data input or output
6	A4	data input or output
7	DIR3	direction control input
8	DIR4	direction control input
9	$\overline{OE}$	output enable input (active LOW)
10	GND	ground (0V)
11	B4	data input or output
12	B3	data input or output
13	B2	data input or output
14	B1	data input or output
15	$V_{CC(B)}$	supply voltage B (Bn pins are referenced to $V_{CC(B)}$)
16	$V_{CC(A)}$	supply voltage A (An, $\overline{OE}$ and DIRn inputs are referenced to $V_{CC(A)}$)

2.4、Function Table

Supply voltage	Input					Input/output	
$V_{CC(A)}$,$V_{CC(B)}$	$\overline{OE}$	DIR1	DIR2	DIR3	DIR4	An	Bn
1.2V to 5.5V	L	L	X	X	X	A1=B1	input B1
1.2V to 5.5V	L	H	X	X	X	input A1	B1=A1
1.2V to 5.5V	L	X	L	X	X	A2=B2	input B2
1.2V to 5.5V	L	X	H	X	X	input A2	B2=A2
1.2V to 5.5V	L	X	X	L	X	A3=B3	input B3
1.2V to 5.5V	L	X	X	H	X	input A3	B3=A3
1.2V to 5.5V	L	X	X	X	L	A4=B4	input B4
1.2V to 5.5V	L	X	X	X	H	input A4	B4=A4
1.2V to 5.5V	H	X	X	X	X	Z	Z
GND[3]	X	X	X	X	X	Z	Z

Note:

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The An, DIRn and $\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The Bn input circuit is referenced to $V_{CC(B)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+6.5	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+6.5	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
input voltage	V_I	-[1]	-0.5	+6.5	V
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output voltage	V_O	Active mode[1][2][3]	-0.5	V_{CCO}+0.5	V
		Suspend or 3-state mode[1]	-0.5	+6.5	V
output current	I_O	V_O=0V to V_{CCO}[2]	-	±50	mA
supply current	I_{CC}	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin	-	100	mA
ground current	I_{GND}	per GND pin	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	260		℃

Note:

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] V_{CCO}+0.5V should not exceed 6.5V.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	1.2	-	5.5	V
supply voltage B	$V_{CC(B)}$	-	1.2	-	5.5	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	Active mode[1]	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	5.5	V
ambient temperature	T_{amb}	-	-40	-	+125	℃
input transition rise and fall rate	Δt/ΔV	V_{CCI}=1.2V[2]	-	-	20	ns/V
		V_{CCI}=1.4V to 1.95V	-	-	20	ns/V
		V_{CCI}=2.3V to 2.7V	-	-	20	ns/V
		V_{CCI}=3.0V to 3.6V	-	-	10	ns/V
		V_{CCI}=4.5V to 5.5V	-	-	5	ns/V

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}[1]	I_O=-3mA; V_{CCO}=1.2V	-	1.09	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=3mA; V_{CCO}=1.2V[1]	-	0.07	-	V
input leakage current	I_I	DIRn, $\overline{OE}$ input; V_I=0V to 5.5V; V_{CCI}=1.2V to 5.5V[2]		-	-	±1	uA
bus hold LOW current	I_{BHL}	A or B port; V_I=0.42V; V_{CCI}=1.2V[2]		-	19	-	uA
bus hold HIGH current	I_{BHH}	A or B port; V_I=0.78V; V_{CCI}=1.2V[2]		-	-19	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port; V_{CCI}=1.2V[2][3]		-	19	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port; V_{CCI}=1.2V[2][3]		-	-19	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[1]		-	-	±1	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[1]		-	-	±1	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[1]		-	-	±1	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±1	uA

		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V	-	-	±1	uA
input capacitance	C_I	DIRn, $\overline{OE}$ input; V_I=0V or 3.3V; $V_{CC(A)}$=3.3V	-	3	-	pF
input/output capacitance	$C_{I/O}$	A and B port; V_O=3.3V or 0V; $V_{CC(A)}$ =$V_{CC(B)}$=3.3V	-	6.5	-	pF

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input[1]	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		DIRn, $\overline{OE}$ input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	data input[1]	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		DIRn, $\overline{OE}$ input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3$V_{CC(A)}$	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V[2]	V_{CCO}-0.1	-	-	V
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IL}[2]	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V

			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
input leakage current	I_I	DIRn, $\overline{OE}$ input;V_I=0V or 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±2	uA
bus hold LOW current	I_{BHL}	A or B port[1]	V_I=0.49V; V_{CCI}=1.4V	15	-	-	uA
			V_I=0.58V; V_{CCI}=1.65V	25	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	100	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
bus hold HIGH current	I_{BHH}	A or B port[1]	V_I=0.91V; V_{CCI}=1.4V	-15	-	-	uA
			V_I=1.07V; V_{CCI}=1.65V	-25	-	-	uA
			V_I=1.70V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-100	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port[1][3]	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port[1][3]	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[2]		-	-	±2	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[2]		-	-	±2	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[2]		-	-	±2	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±2	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±2	uA
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A[1]	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	15	uA
			$V_{CC(A)}$=5.5V;$V_{CC(B)}$=0V	-	-	15	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=5.5V	-2	-	-	uA
		B port;	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to	-	-	15	uA

		V_I=0V or V_{CCI}; I_O=0A	5.5V				
			$V_{CC(B)}$=0V;$V_{CC(A)}$=5.5V	-2	-	-	uA
			$V_{CC(B)}$=5.5V;$V_{CC(A)}$=0V	-	-	15	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	25	uA
additional supply current	ΔI_{CC}	per input; $V_{CC(A)}$,$V_{CC(B)}$= 3.0V to 5.5V	DIRn and $\overline{OE}$ input; DIRn or $\overline{OE}$ input at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	50	uA
			A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open[4]	-	-	50	uA
			B port; B port at $V_{CC(B)}$-0.6V; nDIR at GND; A port=open[4]	-	-	50	uA

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

[4] For non bus hold parts only (AiP74LVC4T774).

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input[1]	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		DIRn, $\overline{OE}$ input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	data input[1]	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		DIRn, $\overline{OE}$ input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V

			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	$0.3V_{CC(A)}$	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V[2]	V_{CCO}-0.1	-	-	V
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IL}[2]	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
input leakage current	I_I	DIRn, $\overline{OE}$ input;V_I=0V or 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±10	uA
bus hold LOW current	I_{BHL}	A or B port[1]	V_I=0.49V; V_{CCI}=1.4V	10	-	-	uA
			V_I=0.58V; V_{CCI}=1.65V	20	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	80	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
bus hold HIGH current	I_{BHH}	A or B port[1]	V_I=0.91V; V_{CCI}=1.4V	-10	-	-	uA
			V_I=1.07V; V_{CCI}=1.65V	-20	-	-	uA
			V_I=1.70V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-80	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port[1][3]	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port[1][3]	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[2]		-	-	±10	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[2]		-	-	±10	uA

		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[2]		-	-	±10	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±10	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±10	uA
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A[1]	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	20	uA
			$V_{CC(A)}$=5.5V;$V_{CC(B)}$=0V	-	-	20	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=5.5V	-4	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	20	uA
			$V_{CC(B)}$=0V;$V_{CC(A)}$=5.5V	-4	-	-	uA
			$V_{CC(B)}$=5.5V;$V_{CC(A)}$=0V	-	-	20	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	30	uA
additional supply current	ΔI_{CC}	per input; $V_{CC(A)}$,$V_{CC(B)}$= 3.0V to 5.5V	DIRn and $\overline{OE}$ input; DIRn or $\overline{OE}$ input at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	75	uA
			A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open[4]	-	-	75	uA
			B port; B port at $V_{CC(B)}$-0.6V; nDIR at GND; A port=open[4]	-	-	75	uA

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

[4] For non bus hold parts only (AiP74LVC4T774).

3.3.4、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$										Unit
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.5V±0.1V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	17.6	-	15.3	-	13.1	-	12.5	-	12.5	ns
		Bn to An	-	17.5	-	16.3	-	15.2	-	14.4	-	13.8	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	29.1	-	29.1	-	29.1	-	29.1	-	29.1	ns
		$\overline{OE}$ to Bn	-	36.4	-	34.5	-	17.3	-	15.5	-	13.6	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	33.6	-	33.6	-	33.6	-	33.6	-	33.6	ns
		$\overline{OE}$ to Bn	-	37.3	-	35.5	-	18.2	-	15.5	-	14.5	ns
$V_{CC(A)}$=1.8V±0.15V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	16.4	-	13.1	-	11.1	-	10.1	-	10.0	ns
		Bn to An	-	15.2	-	12.7	-	11.4	-	10.6	-	10.1	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	29.1	-	28.9	-	28.7	-	28.5	-	28.4	ns
		$\overline{OE}$ to Bn	-	36.4	-	32.9	-	15.5	-	14.5	-	13.0	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	24.5	-	24.5	-	24.4	-	24.3	-	24.3	ns
		$\overline{OE}$ to Bn	-	35.5	-	34.5	-	18.2	-	14.2	-	13.5	ns
$V_{CC(A)}$=2.5V±0.2V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	15.3	-	11.9	-	9.2	-	8.2	-	7.6	ns
		Bn to An	-	13.0	-	10.6	-	8.9	-	7.9	-	7.1	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	10.9	-	10.9	-	10.9	-	10.9	-	10.9	ns
		$\overline{OE}$ to Bn	-	33.6	-	30.5	-	13.6	-	13.0	-	9.9	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	15.5	-	15.5	-	15.5	-	15.5	-	15.5	ns
		$\overline{OE}$ to Bn	-	33.6	-	29.5	-	15.9	-	12.3	-	10.0	ns
$V_{CC(A)}$=3.3V±0.3V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	14.6	-	11.2	-	8.1	-	7.0	-	6.5	ns
		Bn to An	-	12.3	-	9.8	-	7.9	-	6.8	-	6.0	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	10.9	-	10.9	-	10.9	-	10.9	-	10.9	ns
		$\overline{OE}$ to Bn	-	30.9	-	28.2	-	13.2	-	11.4	-	9.5	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	12.3	-	12.3	-	12.1	-	12.0	-	12.0	ns
		$\overline{OE}$ to Bn	-	33.5	-	28.5	-	16.5	-	11.3	-	9.5	ns
$V_{CC(A)}$=5.0V±0.5V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	14.1	-	10.6	-	7.3	-	6.3	-	5.6	ns
		Bn to An	-	12.3	-	9.5	-	7.4	-	6.3	-	5.5	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	ns
		$\overline{OE}$ to Bn	-	32.5	-	29.5	-	12.3	-	10.9	-	8.9	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	9.7	-	9.7	-	9.7	-	9.7	-	9.7	ns
		$\overline{OE}$ to Bn	-	33.5	-	28.5	-	16.7	-	12.3	-	9.7	ns

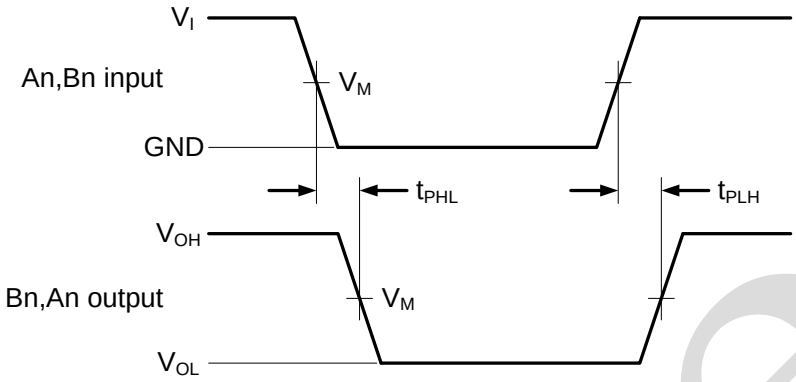
3.3.5、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$										Unit
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.5V±0.1V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	19.4	-	16.8	-	14.4	-	13.8	-	13.8	ns
		Bn to An	-	19.2	-	17.9	-	16.7	-	15.8	-	15.2	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	32	-	32	-	32	-	32	-	32	ns
		$\overline{OE}$ to Bn	-	40	-	38	-	19	-	17	-	15	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	37	-	37	-	37	-	37	-	37	ns
		$\overline{OE}$ to Bn	-	41	-	39	-	20	-	17	-	16	ns
$V_{CC(A)}$=1.8V±0.15V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	18	-	14.4	-	12.2	-	11.1	-	11	ns
		Bn to An	-	16.7	-	14	-	12.5	-	11.7	-	11.1	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	32	-	31.8	-	31.6	-	31.3	-	31.2	ns
		$\overline{OE}$ to Bn	-	40	-	36.2	-	17.1	-	16.0	-	14.3	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	27	-	27	-	26.8	-	26.7	-	26.7	ns
		$\overline{OE}$ to Bn	-	39	-	38	-	20	-	15.6	-	14.8	ns
$V_{CC(A)}$=2.5V±0.2V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	16.8	-	13.1	-	10.1	-	9	-	8.4	ns
		Bn to An	-	14.3	-	11.7	-	9.8	-	8.7	-	7.8	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	12	-	12	-	12	-	12	-	12	ns
		$\overline{OE}$ to Bn	-	37	-	33.6	-	15	-	14.3	-	10.9	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	17	-	17	-	17	-	17	-	17	ns
		$\overline{OE}$ to Bn	-	37	-	32.5	-	17.5	-	13.5	-	11	ns
$V_{CC(A)}$=3.3V±0.3V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	16.1	-	12.3	-	8.9	-	7.7	-	7.2	ns
		Bn to An	-	13.5	-	10.8	-	8.7	-	7.5	-	6.6	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	12	-	12	-	12	-	12	-	12	ns
		$\overline{OE}$ to Bn	-	34	-	31	-	14.5	-	12.5	-	10.4	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	13.5	-	13.5	-	13.3	-	13.2	-	13.2	ns
		$\overline{OE}$ to Bn	-	36.8	-	31.4	-	18.1	-	12.4	-	10.5	ns
$V_{CC(A)}$=5.0V±0.5V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	15.5	-	11.7	-	8	-	6.9	-	6.2	ns
		Bn to An	-	13.5	-	10.5	-	8.1	-	6.9	-	6	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	9.2	-	9.2	-	9.2	-	9.2	-	9.2	ns
		$\overline{OE}$ to Bn	-	35.8	-	32.5	-	13.5	-	12	-	9.8	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	10.7	-	10.7	-	10.7	-	10.7	-	10.7	ns
		$\overline{OE}$ to Bn	-	36.8	-	31.4	-	18.4	-	13.5	-	10.7	ns

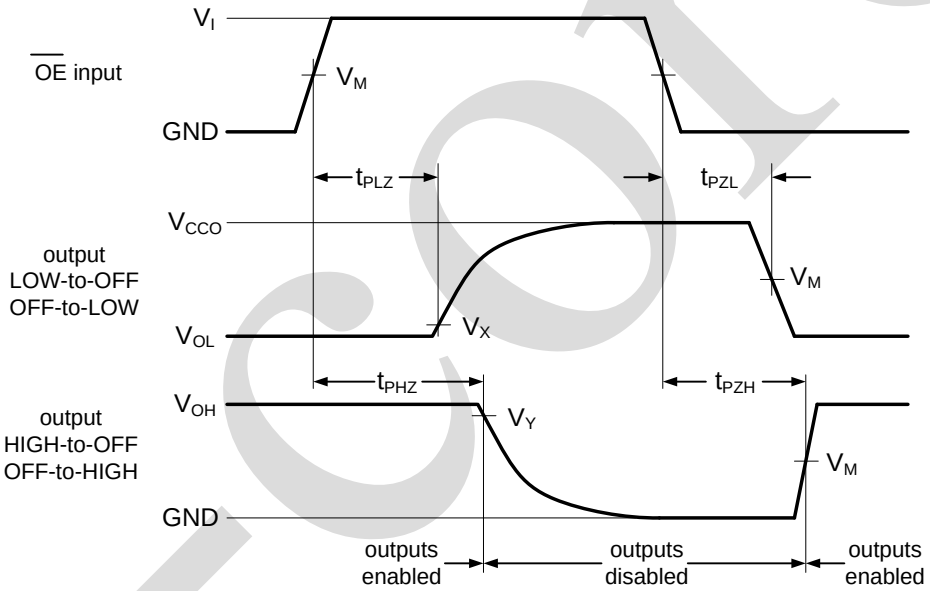
4、Testing Circuit

4.1、AC Testing Waveforms



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. The data input (An, Bn) to output (Bn, An) propagation delay times



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and disable times

4.2、Measurement Points

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}$,$V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.0V to 5.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

4.3、AC Testing Circuit

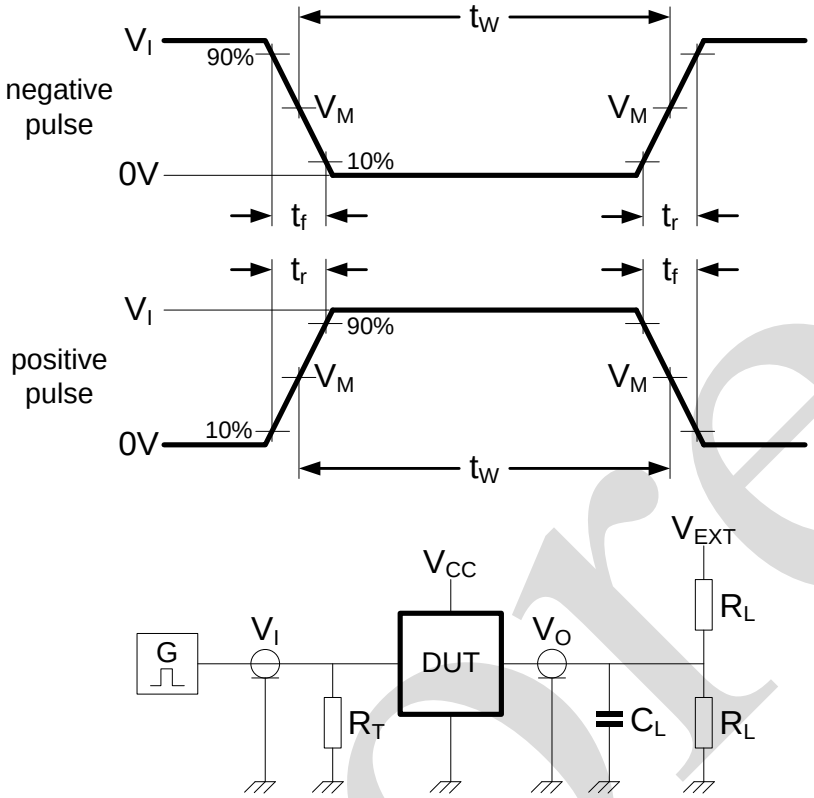


Figure 5. Load circuitry for switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance.

V_{EXT}=External voltage for measuring switching times.

4.4、Test Data

Supply voltage	**Input**		**Load**		**V_{EXT}**		
$V_{CC(A)}$,$V_{CC(B)}$	**V_I[1]**	$\Delta t/\Delta V$[2]	**C_L**	**R_L**	**t_{PLH}, t_{PHL}**	**t_{PZH}, t_{PHZ}**	**t_{PZL}, t_{PLZ}[3]**
1.2V to 5.5V	V_{CCI}	≤1.0ns/V	15pF	2kΩ	open	GND	$2V_{CCO}$

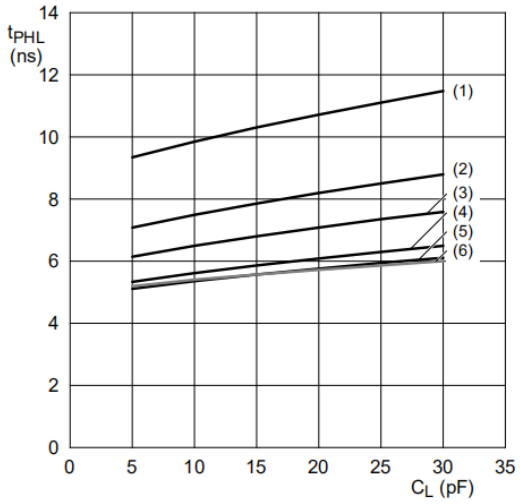
Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

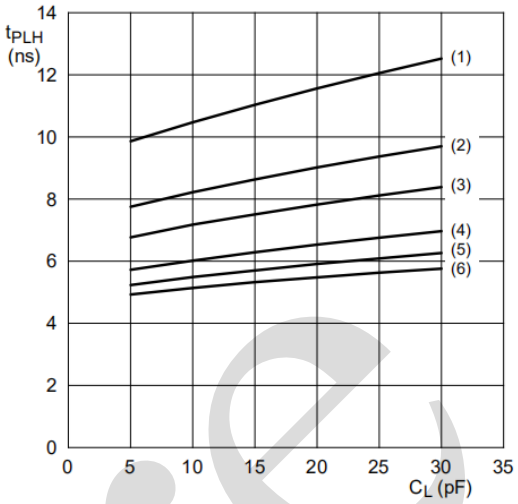
[2] dV/dt≥1.0V/ns.

[3] V_{CCO} is the supply voltage associated with the output port.

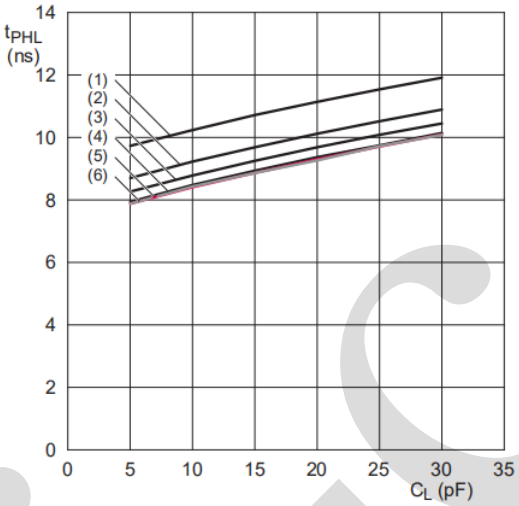
5、Characteristic Curve



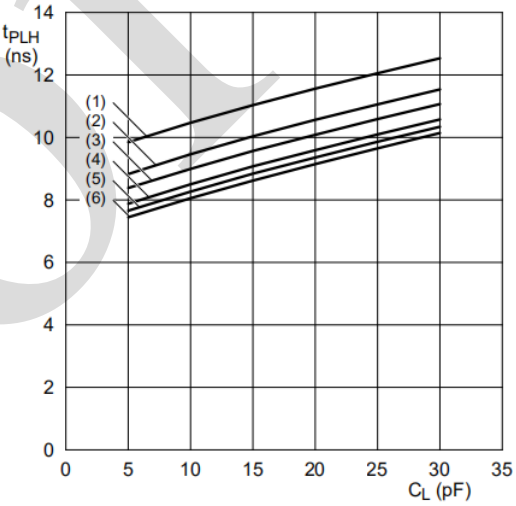
a. HIGH to LOW propagation delay (An to Bn)



b. LOW to HIGH propagation delay (An to Bn)



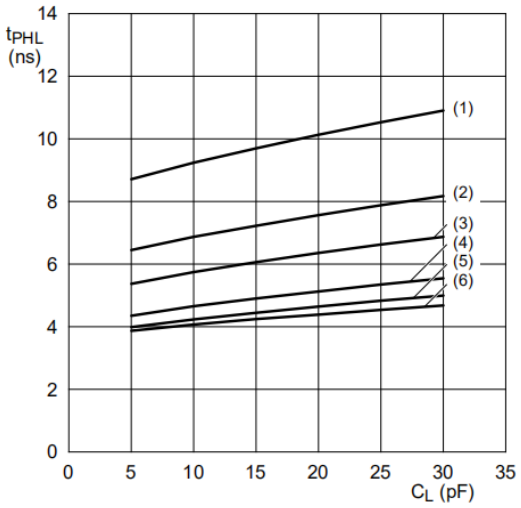
c. HIGH to LOW propagation delay (Bn to An)



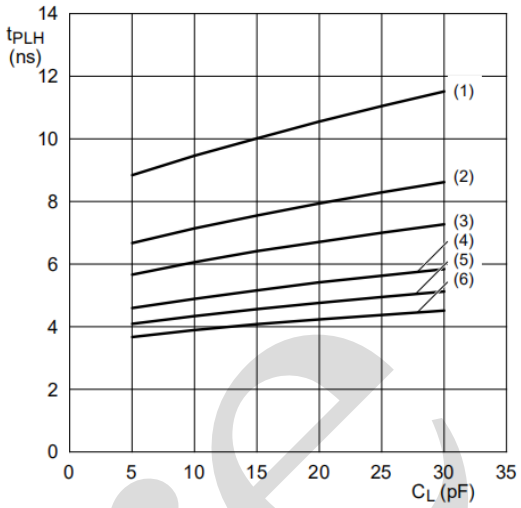
d. LOW to HIGH propagation delay (Bn to An)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

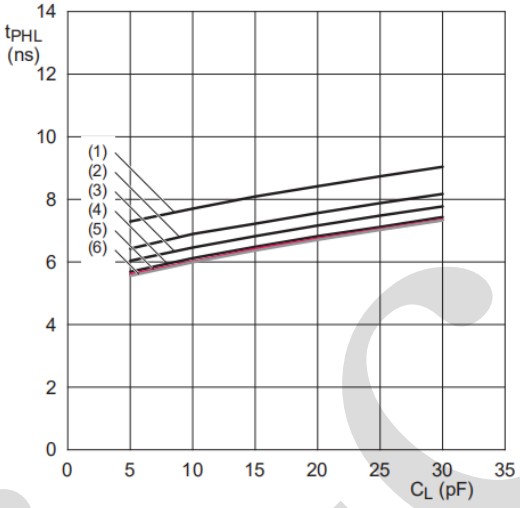
Figure 6. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.2V



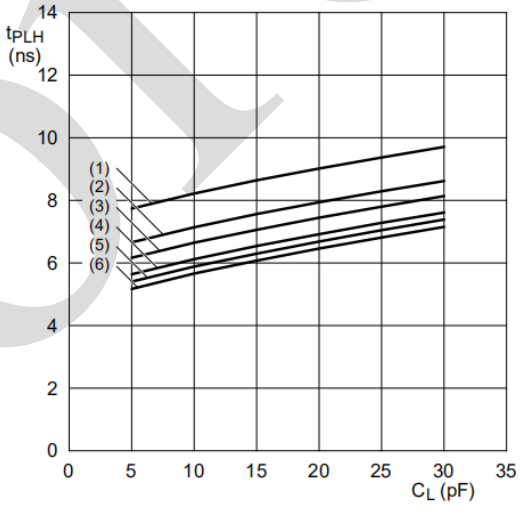
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



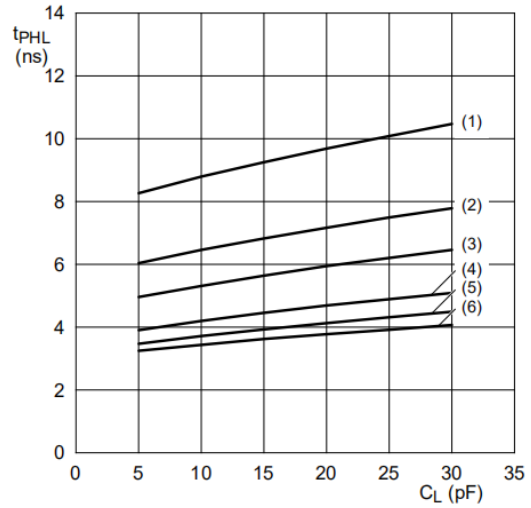
c. HIGH to LOW propagation delay (nBn to nAn)



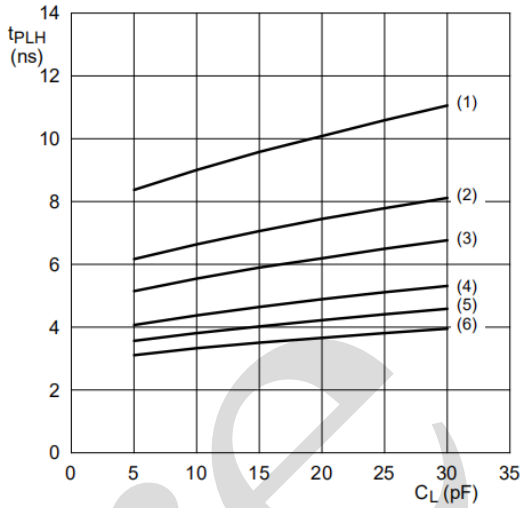
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

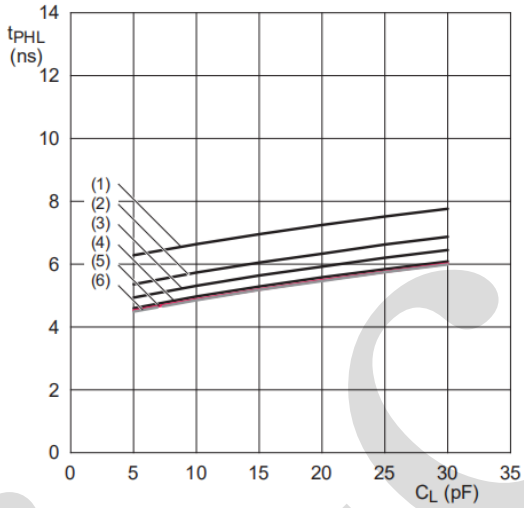
Figure 7. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.5V



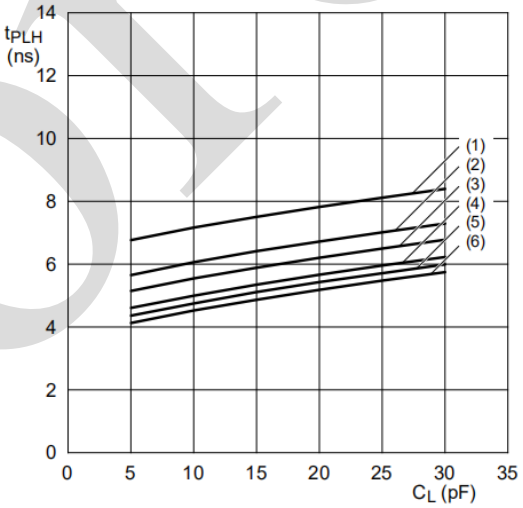
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



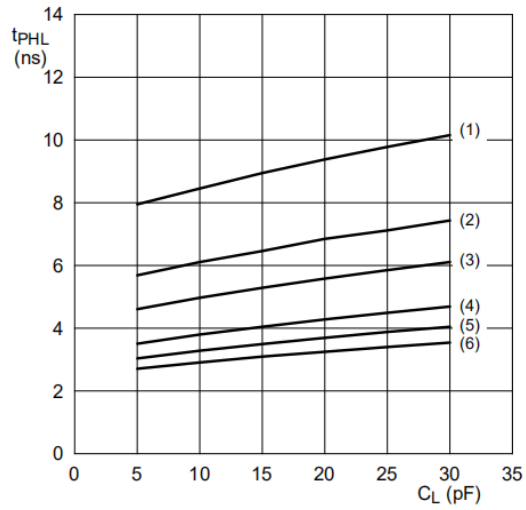
c. HIGH to LOW propagation delay (nBn to nAn)



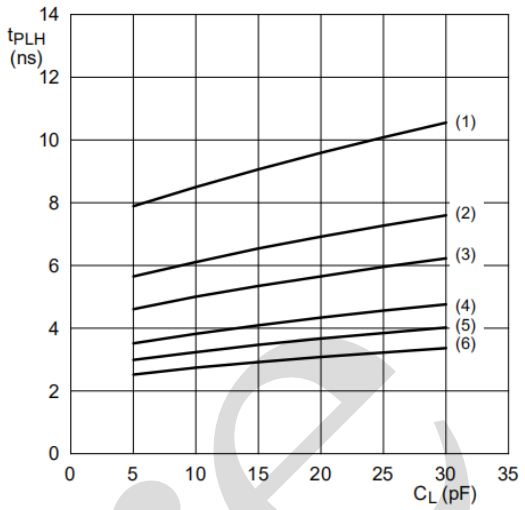
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

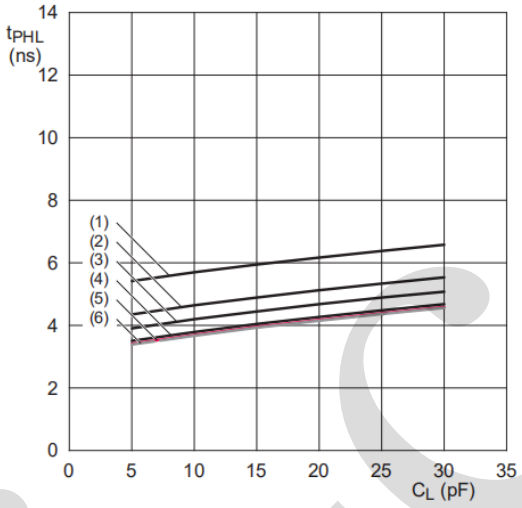
Figure 8. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.8V



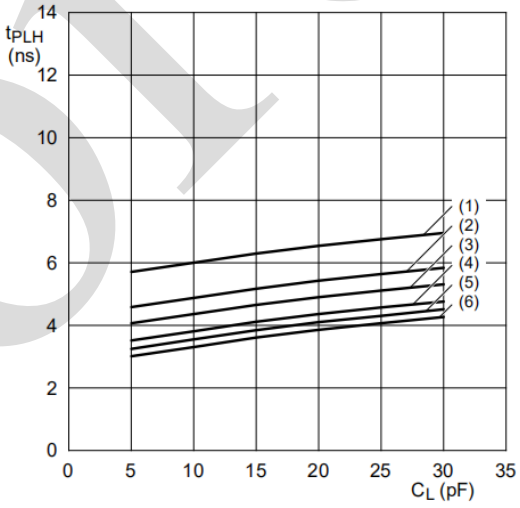
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



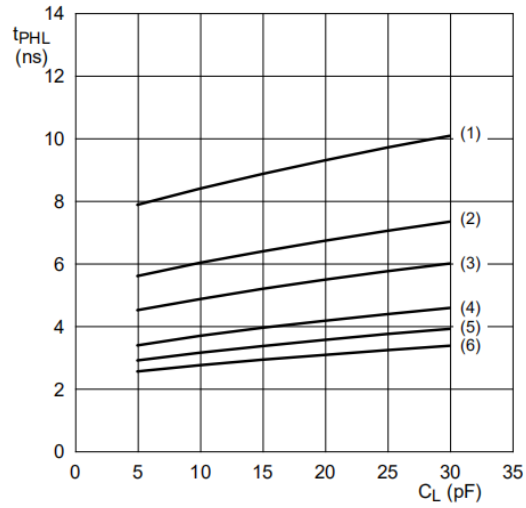
c. HIGH to LOW propagation delay (nBn to nAn)



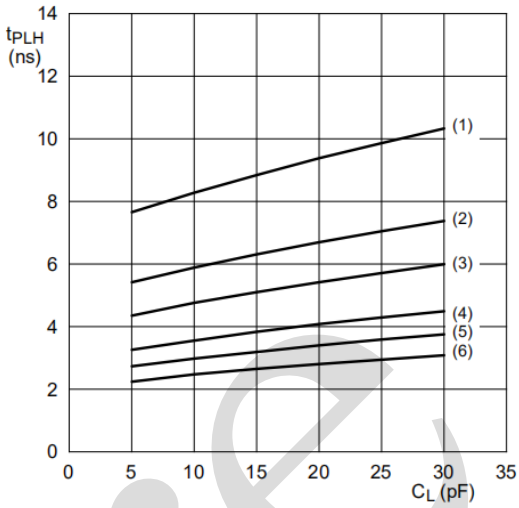
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

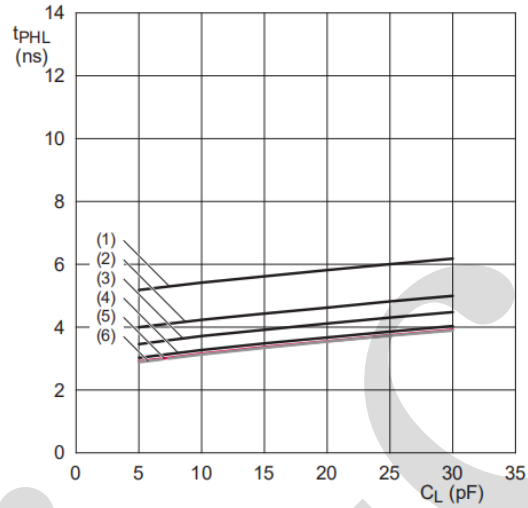
Figure 9. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=2.5V



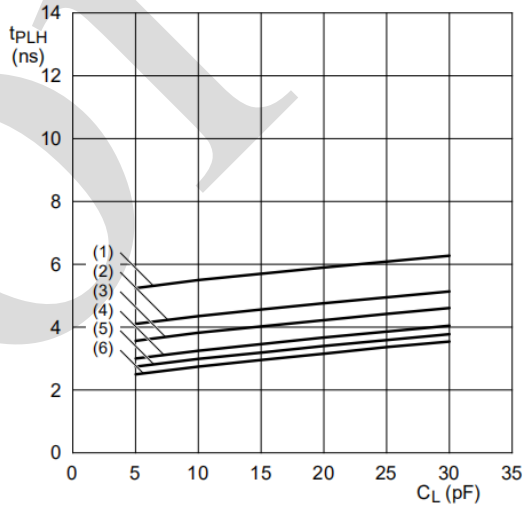
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



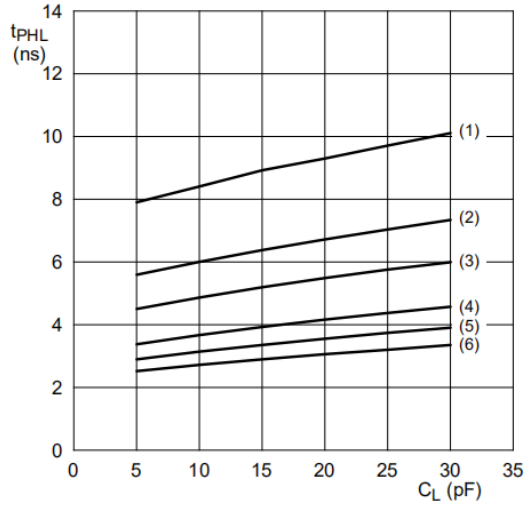
c. HIGH to LOW propagation delay (nBn to nAn)



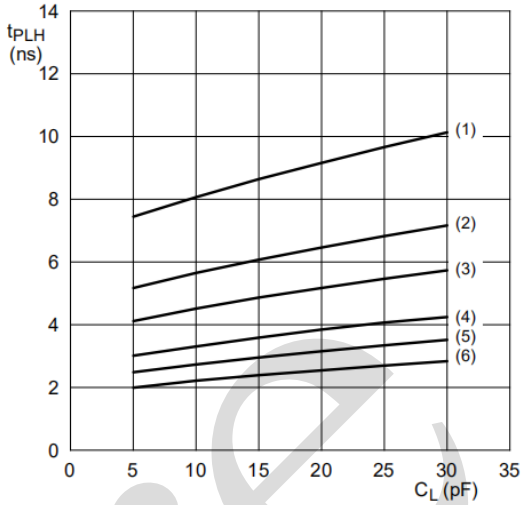
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

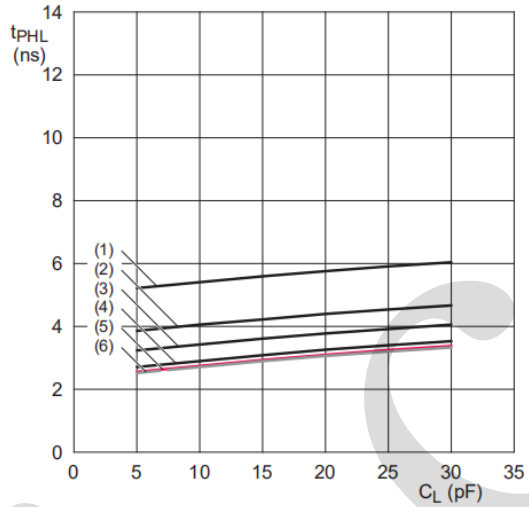
Figure 10. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=3.3V



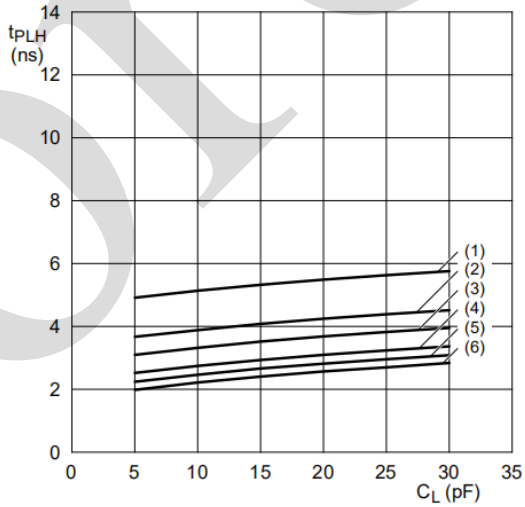
a. HIGH to LOW propagation delay (nAn to nBn)



b. LOW to HIGH propagation delay (nAn to nBn)



c. HIGH to LOW propagation delay (nBn to nAn)



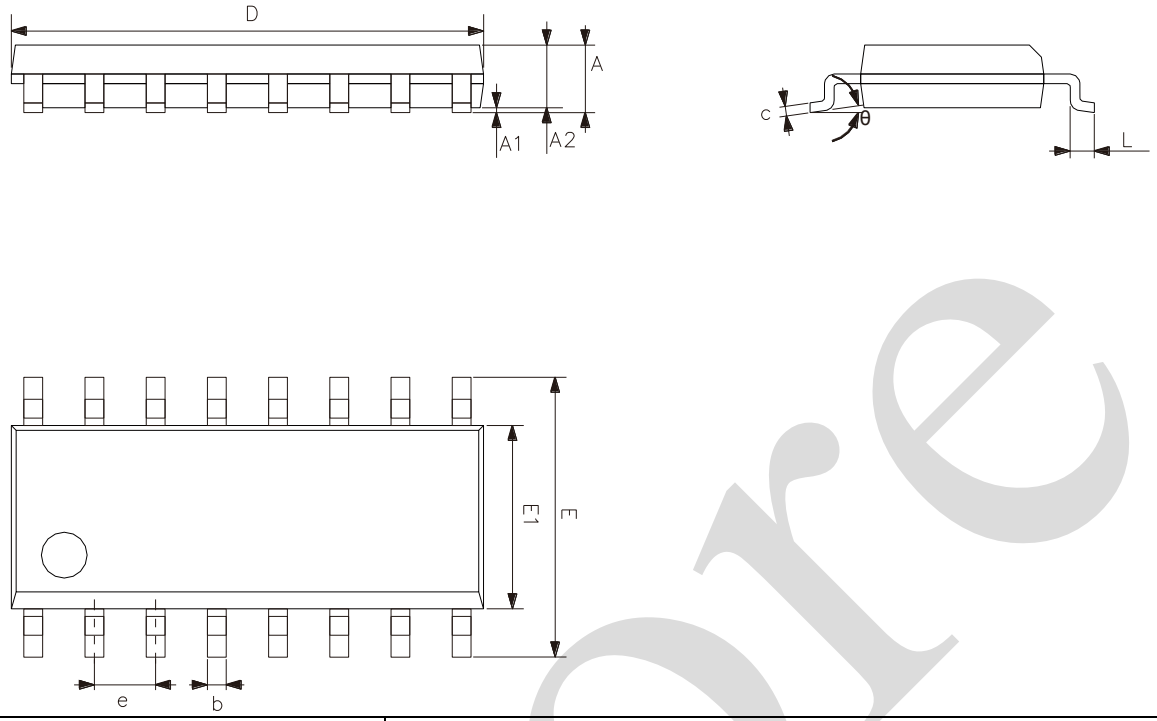
d. LOW to HIGH propagation delay (nBn to nAn)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

Figure 11. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=5.0V

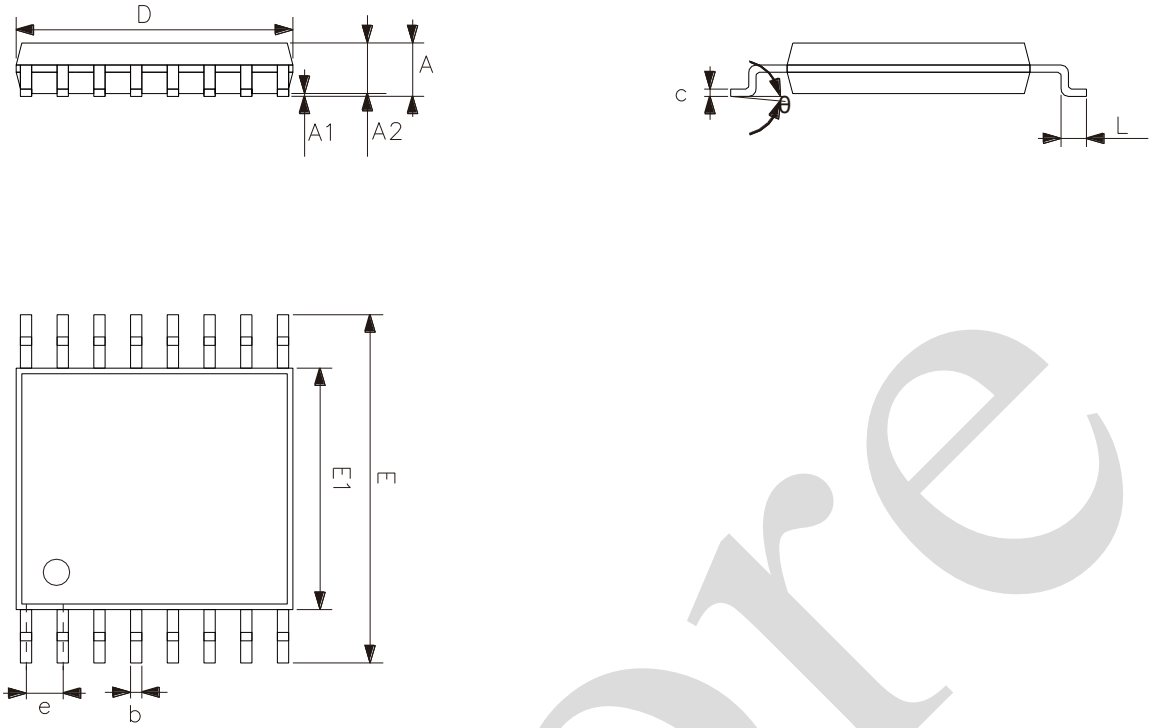
6、Package Information

6.1、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

6.2、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We Recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core's application to avoid failure in the application or the application of the customer' s third party users. I-Core does not accept any liability.

The Company reserves the right to change or improve the information published in this chapter at any time. The information in this chapter are subject to change without notice. We recommend the customer to consult our sales staff before purchasing.

Please obtain related materials form i-Core's regular channels and we are not responsible for its content if it is provided by sources other than our company.

In case of any conflict between the Chinese and English version, the version is subject to the Chinese one.